Reviewer 1

Feedback comment:

AR/Digital Logic and Digital Systems/Multiple representations/layers of interpretation (e.g., hardware is just another layer)

Comment: I'm not sure what they are driving at here. Are they saying that a functional hardware/software hierarchy should be taught? If so, what's with the "Multiple representations"? What is that supposed to involve?

How incorporated: The topic changed to “Functional hardware and software multi-layer architecture”

Why not incorporated:

Date considered: 01 March 2023

Feedback comment:

AR/Digital Logic and Digital Systems/Physical Constraints

Comment: What about the speed of light?

How incorporated: Added speed of light as a new constraint, particularly for new types of interconnect communication, photonics, etc.

Why not incorporated:

Date considered: 01 March 2023

Feedback comment:

Where: AR/Digital Logic and Digital Systems [Illustrative learning outcomes]

Comment: I don't know what "trend temporal diagram" means. The rest of the sentence is gibberish too. "Components that exhibit heterogeneity"? The system is heterogenous because it combines different kinds of components; the individual components do not have to be heterogeneous themselves. Ditto for "inherent parallelism." Why "inherent"? Why not just say "parallelism"? And again, parallelism can be between components, as well as within components.

How incorporated: Learning outcome text changed to Comment on parallelism and data dependencies between and within components in a modern heterogeneous computer architecture.

Why not incorporated:

Date considered: 01 March 2023
Feedback comment:
AR/Digital Logic and Digital Systems [Illustrative learning outcomes]

Comment: this sentence is incredibly wordy. Say it simply: Explain how the "power wall" makes it challenging to harness parallelism.

How incorporated: Text changed to: Explain how the “power wall” makes it challenging to harness parallelism.

Why not incorporated:

Date considered: 01 March 2023

Feedback comment:
AR/Digital Logic and Digital Systems [Illustrative learning outcomes]

- Articulate your ideas on the many equivalent representations of computer functionality, including logical expressions and gates and use mathematical terms to describe the functions of simple combinational and sequential circuits.

Comment: I hope someone else can figure out what this means. I can only guess.

How incorporated: Learning outcome removed, agreed it is too generic.

Why not incorporated:

Date considered: 01 March 2023

Feedback comment:
AR/Digital Logic and Digital Systems [Illustrative learning outcomes]

- Evaluate simple building blocks (e.g., arithmetic-logic unit, registers, movement between registers) of a simple computer design.

Comment: What does "evaluate" mean here? Calculate the speed? Power consumption?

How incorporated: Text changed to “Evaluate power consumption of building blocks (e.g., arithmetic-logic unit, registers, movement between registers) of a simplified computer design.

Why not incorporated:

Date considered: 01 March 2023
Feedback comment:
AR/Digital Logic and Digital Systems [Illustrative learning outcomes]

- Validate the functional and timing diagram behavior of a simple processor.

Comment: Does it mean that the instructions produce correct results? Does it mean that data is given enough time to arrive before it is needed?

How incorporated: Text changed to: Validate the timing diagram behavior of a simple processor, identifying data dependency issues.

Why not incorporated:

Date considered: 01 March 2023

Feedback comment:
AR/Machine-Level Data Representation [Illustrative learning outcomes]

- Follow the diagram and annotate the regions where fixed-length number representations affect accuracy and precision.

Comment: I have no idea what kind of diagram is referred to here.

How incorporated:

Why not incorporated: Text unchanged: Although this learning outcome requires a diagram, it suggests the type of task one might ask their students.

Date considered: 01 March 2023

Feedback comment:
Where: AR/Machine-Level Data Representation [Illustrative learning outcomes]

- Articulate your view on different formats to represent numerical data.

Comment: Asking students their opinion?! For example, is someone expected to say, All numeric data should be represented as floating point? I don’t understand.

How incorporated: The revised Bloom taxonomy indeed stimulates two-way collaboration with students, including asking them their opinion with plausible justifications. The text has been kept, but with a minor change, leading to: Articulate with plausible justification how different formats can represent numerical data.

Why not incorporated:
Feedback comment:
Where: AR/Machine-Level Data Representation [Illustrative learning outcomes]

- Generalize the internal representation of non-numeric data, such as characters, strings, records, and arrays.

Comment: Generalize the internal representation of non-numeric data, such as characters, strings, records, and arrays.

How incorporated: Text changed to: Explain the bit-level representation of non-numeric data, such as characters, strings, records, and arrays.

Why not incorporated:

Feedback comment:
AR/Assembly Level Machine Organization

- Introduction to SIMD vs. MIMD and the Flynn Taxonomy
- Shared memory multiprocessors/multicore organization

Comment: The Flynn taxonomy needs to come before shared-memory multiprocessors.

How incorporated: Changed order of topics.

Why not incorporated:

Feedback comment:
AR/Assembly Level Machine Organization [Illustrative learning outcomes]

- Contextualize the organization of the classical von Neumann machine and its central functional units for embedded system applications.

Comment: Hard to know what this means, or what level of detail is being asked for.

How incorporated: Changed text, making it more specific to cover memory issues (on-chip off-chip) in embedded systems: Contextualize the classical von Neumann functional units in embedded systems, particularly on-chip and off-chip memory.

Why not incorporated:

Date considered: 01 March 2023
Feedback comment:

AR/Assembly Level Machine Organization  [Illustrative learning outcomes]
  ● Articulate features related to different instruction formats, such as addresses per instruction and variable-length vs. fixed-length formats.
  ● Follow a subroutine diagram to comment on how subroutine calls are handled at the assembly level.
Comment: Too vague; what does this mean? This is also too vague. "Follow" and "comment on" are open to many different interpretations.

How incorporated: Text clarified, changed to: Comment on different instruction formats, such as addresses per instruction and variable-length vs fixed-length formats.

Why not incorporated:

Date considered: 01 March 2023

Feedback comment:

AR/Memory Hierarchy  [Illustrative learning outcomes]
Comment: This is badly stated. A DIAGRAM will not reduce memory latency, although an implementation might. If you say "reduces the ... latency," you have to say WHAT it is reduced compared to.

How incorporated: Agreed, the text is confusing. Removed this outcome.

Why not incorporated:

Date considered: 01 March 2023

Feedback comment:

AR/Memory Hierarchy  [Illustrative learning outcomes]
  ● Comment on the principles of memory management.

Comment: What did the authors have in mind here?

How incorporated: Learning outcome text dropped.

Why not incorporated:

Date considered: 01 March 2023
Feedback comment:

AR/Interfacing and Communication/Introduction to communication networks

Comment: I would say that Networking is a Knowledge Area separate from Architecture and Organization. Networking is a separate course in any curriculum I am familiar with.

How incorporated: This topic is very broad, agreed. Topic removed as covered in the networking KU.

Why not incorporated:

Date considered: 01 March 2023

Feedback comment:

AR/Interfacing and Communication [Illustrative learning outcomes]

- Contextualize data access from a magnetic disk drive with solid-state disks.

Comment: A more precise term should be used, e.g., "List advantages of magnetic disks and contrast them with the advantages of solid-state disks."

How incorporated: Suggestion of text accepted: List the advantages of magnetic disks and contrast them with the advantages of solid-state disks.

Why not incorporated:

Date considered: 01 March 2023

Feedback comment:

AR/Interfacing and Communication [Illustrative learning outcomes]

- Comment on standard network organizations like ethernet/bus, ring, switched vs. routed.

Comment: Describe the difference between ...?

How incorporated: Learning outcome removed as the topic “Introduction to networks” has been removed.

Why not incorporated:

Date considered: 01 March 2023
Feedback comment:

AR/Functional Organization  [Illustrative learning outcomes]
   •  Validate alternative implementation of datapaths in modern computer architectures.

Comment: What does "Validate" mean here? How are students expected to perform the validation?

How incorporated:

Why not incorporated: This is an illustrative outcome that would be contextualised with the course material. Validation here needs such context.

Date considered: 01 March 2023

Feedback comment:

AR/Functional Organization  [Illustrative learning outcomes]
   •  Propose a set of control signals using hardwired and microprogrammed implementations.

Comment: Control signals for what?

How incorporated: Learning outcome adjusted to: Propose a set of control signals for adding two integers using hardwired and microprogrammed implementations.

Why not incorporated:

Date considered: 01 March 2023

Feedback comment:

AR/Performance and Energy Efficiency/Branch prediction, Speculative execution, Out-of-order execution

Comment: Tomasulo’s algorithm should probably also be included.

How incorporated: Topic text changed to: Branch prediction, Speculative execution, Out-of-order execution, Tomasulo’s algorithm

Why not incorporated

Date considered: 01 March 2023
Feedback comment:

AR/Performance and Energy Efficiency/Hardware support for multithreading

Comment: A MAJOR omission in this KA is the lack of any mention of concurrency control mechanisms. They are indeed included in "Hardware support for multithreading", but I would expect to see some subtopics like, "Race conditions", "Lock implementations", "Point-to-point synchronization" and "Barrier implementation".

**How incorporated:** Added subtopics under the topic “Hardware support for multithreading” as follows:

- Race conditions
- Lock implementations
- Point-to-point synchronization
- Barrier implementation

**Why not incorporated:**

**Date considered:** 01 March 2023

Feedback comment:

AR/Performance and Energy Efficiency [Illustrative learning outcomes]

- Measure energy savings and performance improvement for a vector processor.

Comment: compared to what?

**How incorporated:** Text changed to: Measure energy savings improvement for an 8-bit integer quantization compared to 32-bits integer quantization.

**Why not incorporated:**

**Date considered:** 01 March 2023

Feedback comment:

AR/Heterogeneous Architectures [Illustrative learning outcomes]

- Contextualize the unique issues multiprocessing systems present concerning memory management and describe how these are addressed.

Comment: Again, I think this term is too vague. You might just ask, “Tell what memory-management issues are found in multiprocessors that are not present in uniprocessors, and how these issues might be
resolved.” (Using the word "addressed" in a sentence about memory management might be ambiguous.)

**How incorporated:** Text adjusted to: Tell what memory-management issues are found in multiprocessors that are not present in uniprocessors and how these issues might be resolved.

**Why not incorporated:**

**Date considered:** 01 March 2023

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**Feedback comment:**

**AR/Heterogeneous Architectures  [Illustrative learning outcomes]**

- Comment on the concept of parallel processing beyond the classical von Neumann model.

Comment: I don't like this at all. "Comment" is vague. Parallel processing FOLLOWS the von Neumann model, in that instructions are still stored in memory along with data.

**How incorporated:** Agreed, the text is too vague. Learning outcome removed.

**Why not incorporated:**

**Date considered:** 01 March 2023

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**Feedback comment:**

**AR/Heterogeneous Architectures  [Illustrative learning outcomes]**

- Document the underlying concept of a domain-specific accelerator in contrast to a general-purpose CPU.

Comment: This is way too vague. You might say something like, Tell how you would determine when to use a domain-specific accelerator instead of just a general-purpose CPU.

**How incorporated:** Text adjusted to: Tell how you would determine when to use a domain-specific accelerator instead of just a general-purpose CPU.

**Why not incorporated:**

**Date considered:** 01 March 2023

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**Feedback comment:**

**AR/Heterogeneous Architectures  [Illustrative learning outcomes]**

- List the design principles of PIM architectures.
Comment: Or, better, List the advantages & disadvantages of PIM...

**How incorporated:** Text adjusted to: List the advantages and disadvantages of PIM architectures.

**Why not incorporated:**

**Date considered:** 01 March 2023

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**Reviewer 2**

**Feedback comment:** High level synthesis is something to add. A relevant topic would be to practice high level hardware description languages such as Chisel. This can be part of AR/Digital Logic and Digital Systems.

**How incorporated:** Added the text to AR/Digital Logic and Digital Systems

- High-level synthesis
  - Register transfer notation
  - Hardware description language (e.g. Verilog/VHDL/Chisel)

**Why not incorporated:**

**Date considered:** 01 March 2023

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**Feedback comment:** I think it might be more relevant to introduce “In-Memory Processing (PIM)” in AR/Memory Hierarchy.

**How incorporated:** Topic In-Memory Processing (PIM) moved to AR/Memory Hierarchy.

**Why not incorporated:**

**Date considered:** 01 March 2023

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**Feedback comment:** In Interfacing and Communication, it would be good to introduce NoC too.

**How incorporated:** Added NoC to AR/ Interfacing and Communication

**Why not incorporated:**

**Date considered:** 01 March 2023

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**Feedback comment:** I don’t see a component where students will have chances to practice the whole SoC design flow from Verilog to layout. I think it is worth to integrate this as I see this as an important skill for students to gain.

**How incorporated:** Added “System-on-chip (SoC) design flow” to AR/Digital Logic and Digital Systems
Feedback comment: It would be good to add a section that describes all the latest packaging/integration solutions such as 3DIC and Chiplets. This can be integrated with Heterogeneous Architectures.

How incorporated: Added new topic to AR/ Heterogeneous Architectures

Why not incorporated:

Date considered: 01 March 2023